EAST SEARCH

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L#	Hits	Search String	Databases
L1	14	US-5541849-$.DID. OR US-5673279-$.DID. OR US-5726985-$.DID. OR US-5893162-$.DID.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L2	2	US-5710934-$.DID.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L3	16	1 or 2	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L4	90	((integrated or digital) adj circuit$1) with (development adj system$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L5	106	(development adj (board or system$1)) with ("IC core" or port$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L6	223	(development adj (board or system$1)) with (core$1 or port$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L7	8	(development adj (board or system$1)) with (core$1 with port$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L8	11	IC core with port$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L9	1	(development adj (board or system$1)) with "IC core"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L10	142	(development adj (board or system$1)) with (core$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L11	106	(development adj (board or system$1)) with (port$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L12	198	(development adj (board or system$1)) with "host"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L13	459	4 or 6 or 12	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L14	7	4 and 12	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L15	40	6 and 12	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L17	33	13 and (configur$5 with core)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L18	2	13 and (translat$5 with RTL with HDL)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L19	15	translat$5 with RTL with HDL	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L21	1	RTL with UTOPIA with interface	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L22	1	RTL with UTOPIA	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L23	1	UTOPIA same RTL	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L24	408	((assign$2 or specif$3) with "clock speed")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L25	1	13 and ((assign$2 or specif$3) with "clock speed")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L26	174	operat$3 with ((assign$2 or specif$3) with "clock speed")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L30	2	13 and (record$2 with (VCD or "Value change dump"))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L33	2	13 and ("test bench")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L34	386	(creat$5 or generat$5 or develop$4) with ("test bench")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L37	25	10 and 11	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L40	1	26 and 27	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L41	1	13 and (("electronically reconfigurable") with (gate near2 array$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L16	8	13 and (HDL near2 (code or software))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L20	20	RTL with signal with port	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L28	5	core with ((assign$2 or specif$3) with "clock speed")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L38	3	24 and 27	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L39	2	13 and 27	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L29	28	13 and (monitor with port$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L27	86	operat$3 with (core with "clock speed")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB

L42	2875	((assign$2 or operat$3) with "clock speed")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L43	5	13 and 42	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L44	2	13 and (monitor near2 port$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L31	3	13 and (VCD or "Value change dump")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L32	29	13 and (("field programmable" or "electronically reconfigurable") with (gate near2 array$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L35	24	((integrated or digital) adj circuit$1) with (creat$5 or generat$5 or develop$4) with ("test bench	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L36	2	13 and ((creat$5 or generat$5 or develop$4) with ("test bench"))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L45	1598	((integrated or digital) adj circuit$1) with verification	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L46	3	45 and (monitor near2 port$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L47	5	UTOPIA and RTL	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L48	6	UTOPIA and HDL	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB

09/778,182 **Michael Scurry**

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Results of search set L10:(development adj (board or system$1)) with (core$1 or port$1) or (development adj (board or system$1)) with "host"

Document	Kind Codes	Title	Issue Date	Current OR	Abstract
US 20030200425	A1	Devices, systems and methods for mode driven stops	20031023	712/229	
US 20030196144	A1	Processor condition sensing circuits, systems and methods	20031016	714/34	
US 20030188221	A1	Method and apparatus for processing control using a multiple redundant processor control sy:	20031002	714/11	
US 20030088710	A1	Simulation environment software	20030508	719/321	
US 20030041166	A1	Method for transmitting data over a physical medium	20030227	709/236	
US 20020095280	A1	Programmable memory emulator capable of emulating unspecified memory devices	20020718	703/24	
US 20020087948	A1	Configurable debug system with proactive error handling	20020704	717/124	
US 20020013918	A1	Devices, systems and methods for mode driven stops	20020131	714/30	
US 20020004933	A1	Configurable debug system with dynamic menus	20020110	717/128	
US 20010042226	A1	System and method for automatically configuring a debug system	20011115	714/39	
US 20010034880	A1	Configurable debug system using source and data objects	20011025	717/128	
US 20010034859	A1	Configurable debug system with wire list walking	20011025	714/39	
US 20010003841	A1	Dual rom microprogrammable microcontroller and universal serial bus microcontroller develop	20010614	712/211	
US 6708290	B2	Configurable debug system with wire list walking	20040316	714/30	
US 6704895	B1	Integrated circuit with emulation register in JTAG JAP	20040309	714/726	
US 6546505	B1	Processor condition sensing circuits, systems and methods	20030408	714/30	
US 6539497	B2	IC with selectively applied functional and test clocks	20030325	714/30	
US 6522985	B1	Emulation devices, systems and methods utilizing state machines	20030218	702/117	
US 6449732	B1	Method and apparatus for processing control using a multiple redundant processor control sy:	20020910	714/12	
US 6370635	B2	Dual ROM microprogrammable microcontroller and universal serial bus microcontroller develc	20020409	712/32	
US 6349392	B1	Devices, systems and methods for mode driven stops	20020219	714/30	
US 6338109	B1	Microcontroller development system and applications thereof for development of a universal s	20020108	710/310	
US 6336195	B1	Method for debugging keyboard basic input/output system (KB-BIOS) in a development notet	20020101	714/34	
US 6188975	B1	Programmatic use of software debugging to redirect hardware related operations to a hardwa	20010213	703/22	

US 6085336 A	Data processing devices, systems and methods with mode driven stops	20000704	714/30
US 6032268 A	Processor condition sensing circuits, systems and methods	20000229	714/30
US 5859993 A	Dual ROM microprogrammable microprocessor and universal serial bus microcontroller devel	19990112	712/208
US 5841670 A	Emulation devices, systems and methods with distributed control of clock domains	19981124	703/23
US 5805792 A	Emulation devices, systems, and methods	19980908	714/28
US 5724505 A	Apparatus and method for real-time program monitoring via a serial interface	19980303	714/45
US 5621651 A	Emulation devices, systems and methods with distributed control of test interfaces in clock do	19970415	703/23
US 5615331 A	System and method for debugging a computing system	19970325	714/9
US 5590349 A	Real time programmable signal processor architecture	19961231	712/36
US 5535331 A	Processor condition sensing circuits, systems and methods	19960709	714/45
US 5524244 A	System for dividing processing tasks into signal processor and decision-making microprocess	19960604	717/140
US 5471636 A	Software development system and method of using same	19951128	717/100
US 5329471 A	Emulation devices, systems and methods utilizing state machines	19940712	703/23
US 5287511 A	Architectures and methods for dividing processing tasks into tasks for a programmable real ti	19940215	717/106
US 5251150 A	Sub-modular development system for modular computer-based instruments	19931005	702/127
US 20040030870 A	Execution of instructions in processor, involves providing instruction field containing halt ident	20040212	